Process (Core/IO)	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Technology	2021 Shuttle Code/Fab/Process Availability											
22nm (1P11M2T2A)	L222101 FAB12A			L222104 FAB12A		L222106 FAB12A			L222109 FAB12A			L222112 FAB12A
ULP/ULL (0.8V/1.8V, 0.8V/2.5V + ULVT/LVT/SVT/HVT/UHVT/EHVT) (SP SRAM / LL SRAM)	✓			✓		✓			✓			✓
28nm (1P11M2T2A)	L282101 FAB12A		X282103 USCXM		L282105 FAB12A		X282107 USCXM				L282111 FAB12A	X282112 USCXM
HLP (1.05V/1.8V, 1.05V/2.5V + LVT/RVT/HVT)(*1)	✓		✓		✓		✓				✓	✓
HPC+ (0.9V/1.8V, 0.9V/2.5V + uLVT/LVT/RVT/HVT/uHVT/eHVT)	✓		✓		✓		✓				✓	✓
HPC (0.9V/1.8V, 0.9V/2.5V + uLVT/LVT/RVT/HVT/uHVT)	✓		✓		✓		✓				✓	✓
EHV (1.0V/8V(+/-)10V)	✓		✓		✓		✓				✓	✓
LPT (1.05V/1.8V + LVT/RVT)	✓		✓		✓		✓				✓	✓
40nm (1P11M2T2H)		X402102 USCXM	S402103 FAB12i		L402105 FAB12A	X402106 USCXM		S402108 FAB12i	L402109 FAB12A	X402110 USCXM		S402112 FAB12i
40nm EFLASH(1.1V/0.9V LVT/RVT/HVT + 0.9V eLVT/eHVT + 2.5V (2.5V/OD3.3V/UD1.8V + 12V (12V/UD5V))			✓									✓
40nm HV :(core1.1V/(IO: 6V HV:32V),(IO: 8V HV:32V),(IO: 8V HV:20V))		✓	✓		✓	✓		✓	✓	✓	✓	
40LP (1.1V / 1.8V(UD1.5V), 2.5V(UD1.8V/OD3.3V))		✓	✓		✓	✓		✓	✓	✓		
40uLP [1.1V/0.9V (uLVT/LVT/RVT/HVT) + 2.5V(UD_1.8V/OD_3.3V) + 0.9V(eHVT eLVT]		✓	✓		✓	✓		✓	✓			✓
55/65nm (1P10M2T2F)	S652101 FAB12i	X552102 USCXM	S652103 FAB12i	L552104 FAB12A	S652105 FAB12i		S652107 FAB12i	X552108 USCXM	L552109 FAB12A	S652110 FAB12i	X552111 USCXM	
65nm SP (1.0V/ 2.5V, 3.3V) (*2)	✓		✓		✓		✓		✓	✓		
65nm LL (1.2V/ 1.8V, 2.5V(OD_3.3V) , 3.3V) (*3)	✓		✓		✓		✓		✓	✓		
65nm LP (1.2V/ 2.5V(UD_1.8V/OD_3.3V)) (*4)	✓		✓		✓		✓		✓	✓		
65nm LL URAM (1.2V/ 2.5V(OD_3.3V), 3.3V)												
55nm SP (1.0V / 2.5V(OD_3.3V), 3.3V)	✓		✓	✓	✓		✓		✓	✓		
55nm LP (1.2V / 2.5V(UD_1.8V / OD_3.3V))	✓		✓	✓	✓		✓		✓	✓		
55nm ULP(0.9~1.2V/2.5V(UD1.8V/OD3.3V))	✓			✓	✓				✓	✓		
55nm HV (1.2V / 6V(UD_5.5V , UD_3.3V) / 32V(+/-16V) + 16V(+/-8V))	✓		✓	✓	✓		✓		✓	✓		
55nm RFSOI (1.2V / 2.5V(UD_1.8))			✓				✓					
55nm EFLASH (1.2V (LVT/RVT/HVT/uHVT) + 2.5V(UD_1.8V/OD_3.3V) + HV_UD_5V)	✓	✓			✓			✓		✓	✓	
90nm (1P9M2T1F)									S902109 FAB12i			
90N (1.0V,1.2V / 1.8V , 2.5V(OD_3.3V) , 3.3V)									✓			

Process						
80HV (1.2V/6V/32V(+/-16V))					√	
90N RF SOI (1.2V/3.3V)					√	
0.11um for AL (1P8M2T)	A112101 FAB8C	A112103 FAB8S	A112105 FAB8C	A112107 FAB8S	A112109 FAB8C	A112111 FAB8S
110AE	√	√	√	√	√	√
110AE EFLASH	√	√	√	√	√	√
110BCD	8C/8D	8C/8D	8C/8D	8C/8D	8C/8D	8C/8D
110BCD+ESF	8D	8D	8D	8D	8D	8D
0.11/0.13um (1P8M2T)		M132104 FAB8D			M132110 FAB8D	
130E Logic (1.2V/ 3.3V)		√			√	
130 MM/RF(1.2V/ 3.3V)		√			√	
L110E (1.2V/ 3.3V)		√			√	
0.11/0.13/0.15/0.162um (1P7M)	L152102 FAB8F	L152104 FAB8S		L152107 FAB8S	L152110 FAB8F	L152112 FAB8S
0.11um HV (1.5V/5.5V/(+/-)16V)	8F/8S	8F/8S		8F/8S	8F/8S	8F/8S
0.13um HV (1.5V/6V/(+/-)16V)	8F/8S/8C	8F/8S/8C		8F/8S/8C	8F/8S/8C	8F/8S/8C
0.15um LL (1.5V/ 3.3V)	8F/8C	8F/8C		8F/8C	8F/8C	8F/8C
0.15um SP (1.5V/ 3.3V)	8F/8C	8F/8C		8F/8C	8F/8C	8F/8C
HV15 large panel (1.8V ; 13.5V ; 19V)	8F/8C	8F/8C		8F/8C	8F/8C	8F/8C
HV15 large panel (1.8V/ 9V ; 13.5V)	8S	8S		8S	8S	8S
0.153um MM (1.8V/3.3V)	8F/8S/8C	8F/8S/8C		8F/8S/8C	8F/8S/8C	8F/8S/8C
0.153um MM (1.8V/5V)	8F	8F		8F	8F	8F
0.153um LL (1.8V/ 3.3V)	8F/8S/8C	8F/8S/8C		8F/8S/8C	8F/8S/8C	8F/8S/8C
0.162um HV (3.3V/16.5V)	8C	8C		8C	8C	8C
0.162um LogicGII (1.8V/3.3V)	8F/8S/8C	8F/8S/8C		8F/8S/8C	8F/8S/8C	8F/8S/8C
0.162um LL (1.8V/3.3V)	8F/8S/8C	8F/8S/8C		8F/8S/8C	8F/8S/8C	8F/8S/8C
0.162um HV (1.8V/5.5V/(+/-)16V)	8F/8S/8C	8F/8S/8C		8F/8S/8C	8F/8S/8C	8F/8S/8C
0.18um (1P6M)	M182102 FAB8C		M182105 FAB8S	M182108 FAB8S		M182111 FAB8C
BCD (1.8/5V) + HV (16-60V)	√		8C	8C		√
MM/RF (1.8V/ 3.3V)	√		8C	8C		√
LL+ MMC (1.8V/ 3.3V)	√		√	√		√
LogicGII + MMC (1.8V/ 3.3V)	√		√	√		√
0.18um (1P6M) :						F182112 Fab8E

eFlash	√										√
0.5um/0.35um/0.3um/0.25um(*4) (2P3M)			P352103 FAB8AB						P352110 FAB8AB		
CDMOS / FDMOS (30V , 800V)			√						√		
0.3um/0.25um BCD (*5)			√						√		
0.35um MM			√						√		

Notes：

　*1 : (12A) shall depend on reservation ratio to decide if provide, subject to change after

　kick-off.

　*2 : (12i) LVT, MIM, 6X development in progress, pls contact account manager

　*3 : (12i) 6X development in progress, pls contact account manager

　*4 : (12i) MIM, 6X development in progress, pls contact account manager

　*5 : 0.25um" is merely for "BCD" not for other standard STI process

* : The shuttle will be launched regularly if the minimum number of paidseats has been achieved. Otherwise, any adjustments to the schedule of planned shuttles will be subject to UMCs discretion.

M：Indicates maskallows formix-match among Fabs. Please note that in these cases, the wafer-Qutschedule of the 2nd Fab will be delayed by two weeks (domastic Fabsy four weeks (overseas Fåb)

　following the original schedule of the leading Fab.