SMIC MPW Shuttle Schedule

MPW Notice To serve all customers smoothly, following items must be noticed:

1. Only standard Process/Layers products can attend MPW. No bumping, No Bank and No Corner Split allowed.
2. On one shuttle, 4 seats (including sub-chip in one seat) are the maximum that one customer can get.
3. **MPW only provides 50 dies for function verification.**
4. Shuttles are subject to cancellation if there are not enough passengers on board.
5. Without completion of below items before shuttle start date, shuttle reservation will not be held!

*Quotation should be ready/ DRC must be clean/ SMIC IP merge case must be closed (related information need to be submitted at least 3 days before shuttle start date)

*GDSII and tape out forms all need to be Approved by mask shop/ PTOS should be Approved

6. SMIC dicing size limit: 1500um < X < 12000um, 1500um < Y < 12000um.
7. For 300mm shuttle, suggest use metal scheme condition: 6(M1-M6)+TM1(9kA)+TM2(9kA)+14.5kA ALPA+12mil BG.
8. Overdue MPW booked cases will be cancelled within 90 days after shuttle start.

Tech Node	IO Voltage/Tech Type/Char	CMOS RF	2021 MPW Booking Cut-Off Date											
			Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
28nm	IO=1.8V | IO=2.5V **CMOS Logic (HP)**	**Y**	12 Q7L (Fab2)				4 Q80 (Fab2)				7 Q8F (Fab2)			7 Q8S (Fab2)
40nm	IO=2.5V **CMOS Logic (LL|UP)**	**Y**			9 Q7T (Fab2)		18 Q82 (Fab2)			3 Q8B (Fab2)		26 Q8M (Fab2)		21 Q8T (Fab2)
	IO=8/32V **CMOS High Voltage (HV)**		19 Q7P (Fab2)					8 Q84 (Fab2)						
	IO=1.8V| IO=2.5V **Adv. Emb-Flash (Cu-BEOL with AL-TM2 + RDL process) (LL)**						11 Q81 (Fab2)						9 Q8P (Fab2)	
55nm	IO=2.5/5V | IO=2.5V **Adv. Emb-Flash (Cu-BEOL) (LL)**					6 Q7W (Fab2)							2 Q8N (Fab2)	
	IO=1.8/2.5V | IO=1.8V| IO=2.5V **CMOS Logic (LL)**	**Y**	5 Q7M (Fab2)			13 Q7Z (Fab2)			13 Q88 (Fab2)			19 Q8L (Fab2)		
	IO=6/32V | IO=8/32V **CMOS High Voltage (HV)** **Do not support 2XTM(STM)**													
0.11um	IO=3.3V **Adv. Emb-Super flash (AL-BEOL) (LL)**							15 Q86 (Fab1)						14 Q8U (Fab1)
0.13um	IO=3.3/5V| IO=5V **Adv. Emb-EEPROM (Cu-BEOL) (LL)**				2 Q7S (Fab1)					10 Q8E (Fab1)				
0.11/0.13um	IO=3.3V **CMOS Logic (GE)|Mixed Signal (GE)**	**Y**		23 Q7Q (Fab1)		6 Q7X (Fab1)		1 Q85 (Fab1)		17 Q8D (Fab1)		12 Q8J (Fab1)		28 Q8K (Fab1)
0.153um	IO=3.3V **CMOS Logic (GE)|Mixed Signal (GE)**	**Y**								10 Q8C (Fab1)				
0.18um	IO=5 **BCD V3E (EP)**		12 Q7N (Fab7)			13 Q7Y (Fab1)			20 Q89 (Fab7)				9 Q8Q (Fab1)	
0.18um	IO=3.3V **CMOS Logic (GE)|Mixed Signal (GE)**	**Y**		23 Q7R (Fab1)			25 Q83 (Fab1)				14 Q8G (Fab1)			
	IO=3.3V **CMOS Logic (GE)|Mixed Signal (GE)** IO=5/10/12/20/35/40V **BCDM (BCDM do not support RF)**	**Y**			16 Q7U (Fab7)				6 Q87 (Fab7)				16 Q8R (Fab7)	
	IO=3.3/5V| IO=5V **EEPROM Embedded (GE)**				23 Q7V (Fab1)						14 Q8H (Fab1)			